Description

650V N-CHANNEL ENHANCEMENT MODE POWER MOSFET

Features

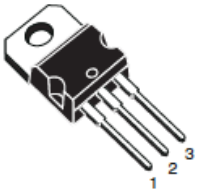
V_{DSS}	$R_{DS(ON)}$ @ 10V (typ)	I_D
650V	1.29Ω	6 A

- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

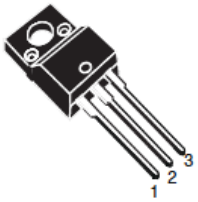
Application

- DC-DC & DC-AC Converters
- Uninterruptible Power Supply (UPS)
- Switch Mode Low Power Supplies

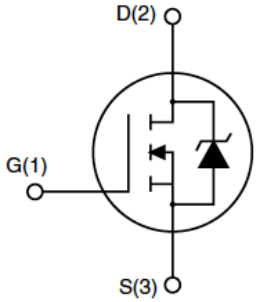
Package



TO-220
G7N65



TO-220F
G7N65



Absolute Maximum Ratings T_C=25℃ unless otherwise specified

Symbol	Parameter		Max.		Units
			TO-220	TO-220F	
V_{DSS}	Drain-Source Voltage		650		V
V_{GSS}	Gate-Source Voltage		± 30		V
I_D	Continuous Drain Current	T_C = 25℃	6	6*	A
		T_C = 100℃	3.79	3.79*	A
I_{DM}	Pulsed Drain Current note1		24	24*	A
E_{AS}	Single Pulsed Avalanche Energy note2		180		mJ
dv/dt	Peak Diode Recovery Energy note3		6		V/ns
P_D	Power Dissipation	T_C = 25℃	110	50	W
	Linear Derating Factor	T_C > 25℃	0.89	0.4	W/℃
$R_{\theta JC}$	Thermal Resistance, Junction to Case		1.12	2.5	℃/W
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150		℃

*Drain current limited by maximum junction temperature

Electrical Characteristics T_C=25℃ unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS} = 0V,I_D = 250mA	650	-	-	V
$\triangle V_{(BR)DSS}$ /$\triangle T_J$	Breakdown Voltage Temperature Coefficient	Reference to 25℃, I_D = 250μA	-	0.5	-	V/℃
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 650V, V_{GS} = 0V	-	-	1	μA
		V_{DS} = 520V, T_C = 125℃	-	-	10	μA
I_{GSS}	Gate to Body Leakage Current	V_{DS} = 0V, V_{GS} = ±30V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage note4	V_{DS} = V_{GS}, I_D = 250μA	2	-	4	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} =10V, I_D = 6A	-	1.29	1.43	Ω
g_{FS}	Forward Transconductance	V_{DS} =30V, I_D = 6A	-	10	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1.0MHz	-	847	-	pF
C_{oss}	Output Capacitance		-	87	-	pF
C_{rss}	Reverse Transfer Capacitance		-	12	-	pF
Q_g	Total Gate Charge	V_{DD} = 520V, I_D = 6A, V_{GS} = 10V	-	23.5	-	nC
Q_{gs}	Gate-Source Charge		-	3.05	-	nC
Q_{gd}	Gate-Drain(“Miller”) Charge		-	10.66	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 320V, I_D = 6A, R_G = 5Ω, V_{GS} = 10V	-	8.2	-	ns
t_r	Turn-On Rise Time		-	14.2	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	31.2	-	ns
t_f	Turn-Off Fall Time		-	24.8	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	6	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	24	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0V, I_S = 6A	-	-	1.5	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0V, I_F = 6A, di/dt =100A/μs	-	254	-	ns
Q_{rr}	Reverse Recovery Charge		-	2.1	-	uC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature

2. L = 10mH, I_{AS} = 6A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C

3. I_{SD} ≤ 6A, di/dt ≤ 200A/μs, V_{DD} ≤ B_{VDSS}, Starting T_J = 25°C

4. Pulse width ≤ 300μs; duty cycle ≤ 2%.

Typical Performance Characteristics

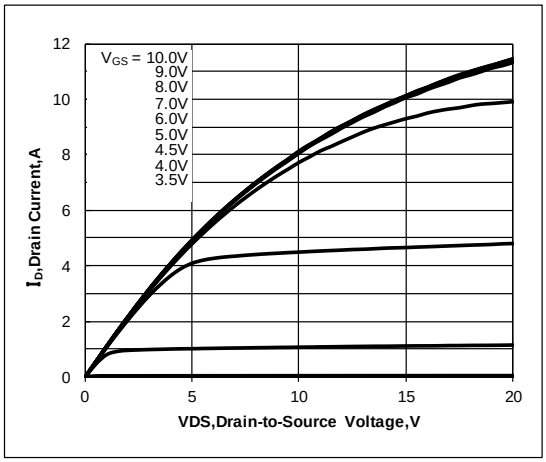


Figure 1. Output Characteristics

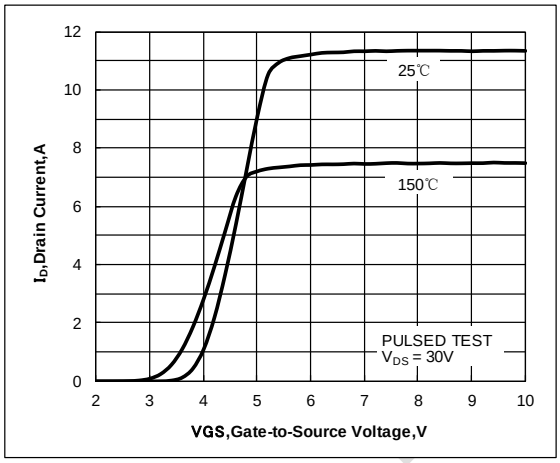


Figure 2. Transfer Characteristics

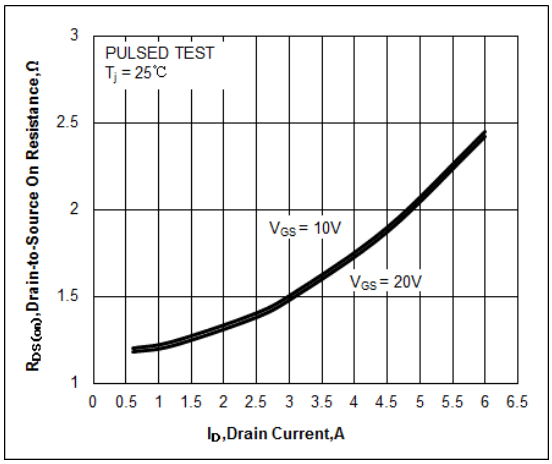


Figure 3. Drain-to-Source On Resistance vs. Drain Current and Gate Voltage

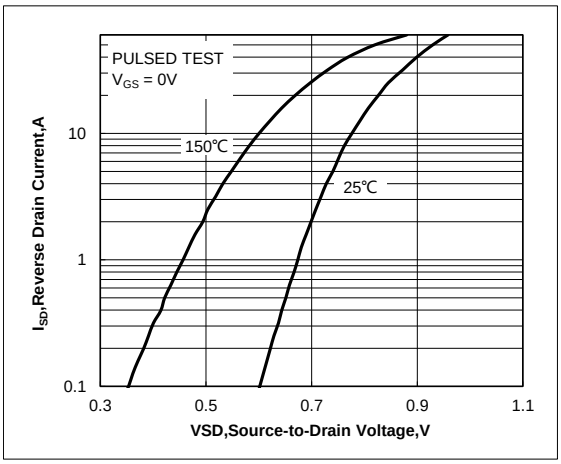


Figure 4. Body Diode Forward Voltage vs. Source Current and Temperature

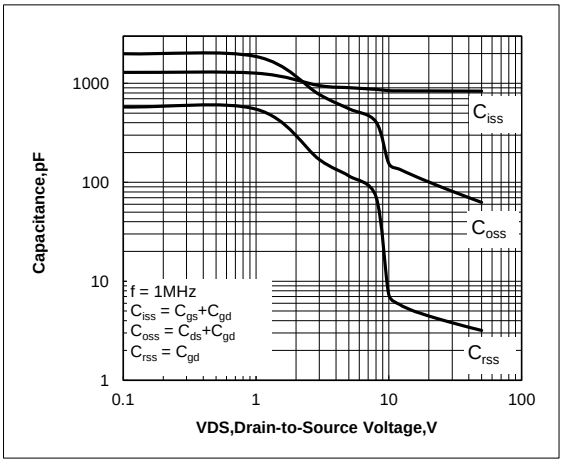


Figure 5. Capacitance Characteristics

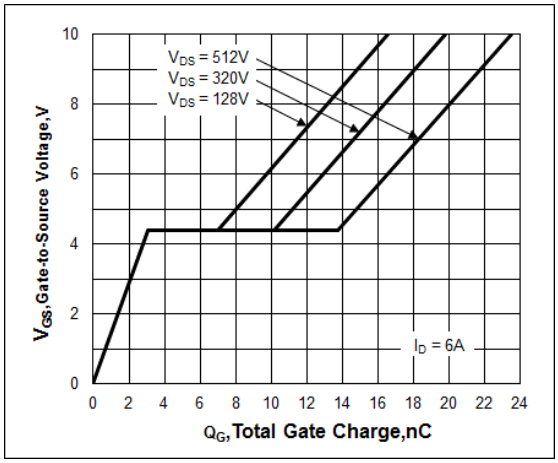


Figure 6. Gate Charge Characteristics

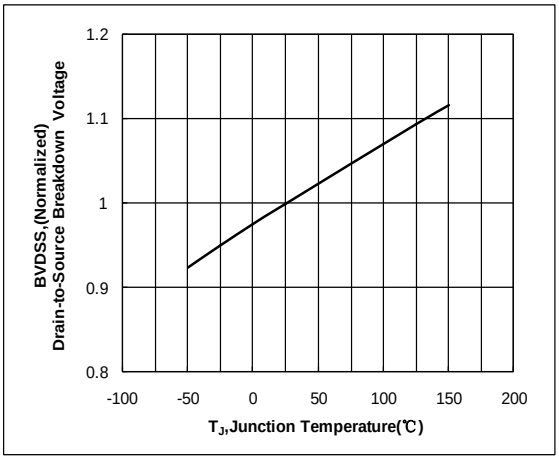


Figure 7. Normalized Breakdown Voltage vs. Junction Temperature

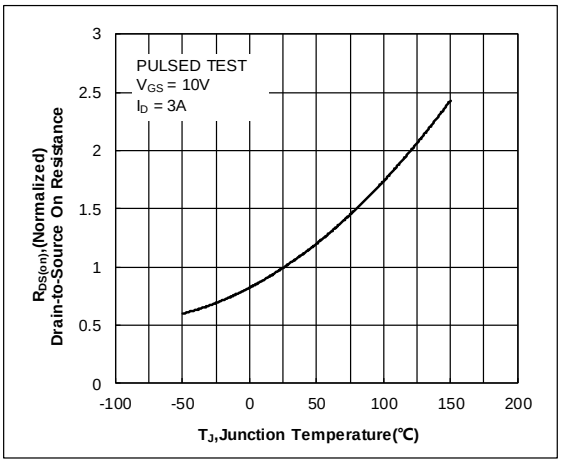


Figure 8. Normalized On Resistance vs. Junction Temperature

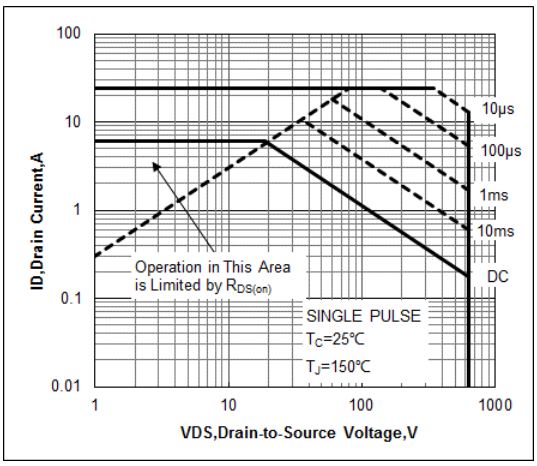


Figure 9. Maximum Safe Operating Area

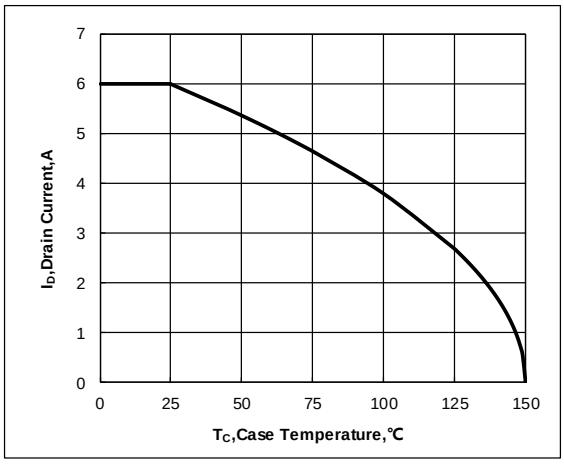


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

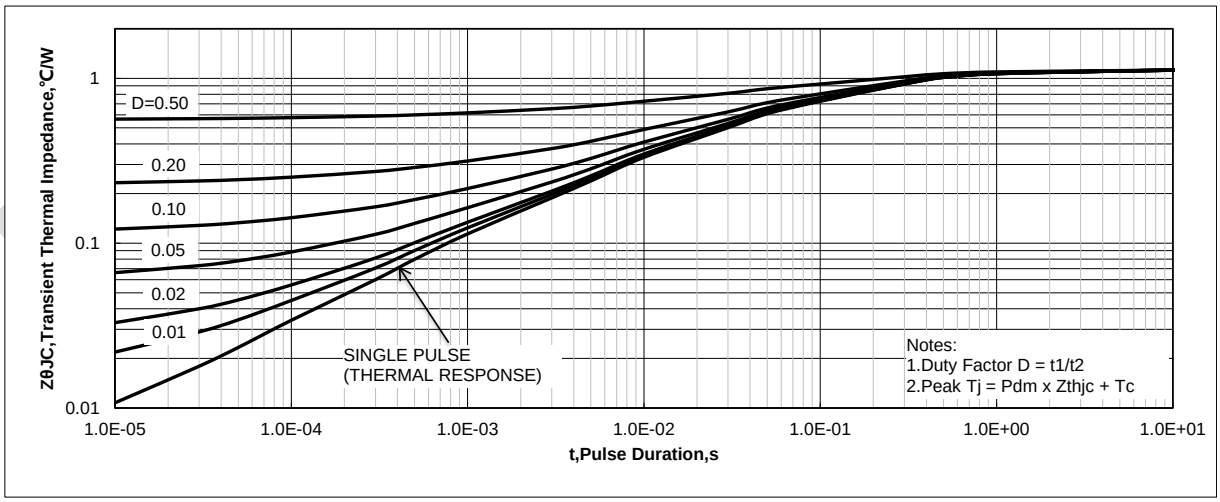


Figure 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

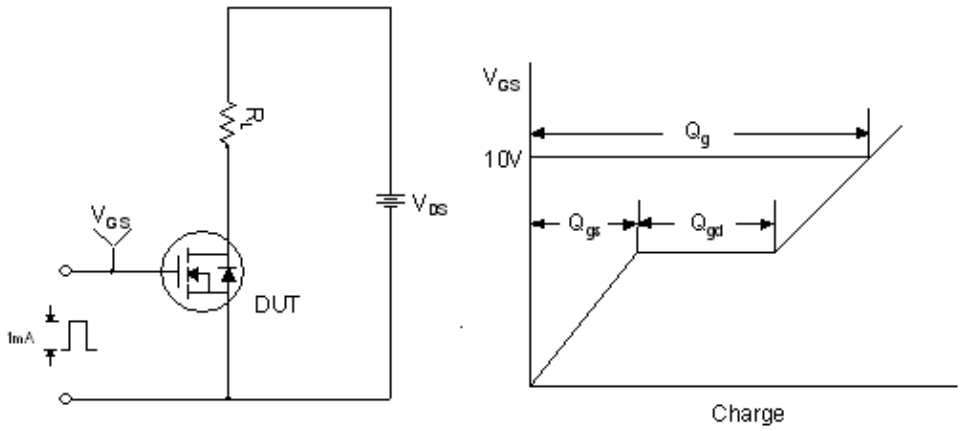


Figure 12. Gate Charge Test Circuit & Waveform

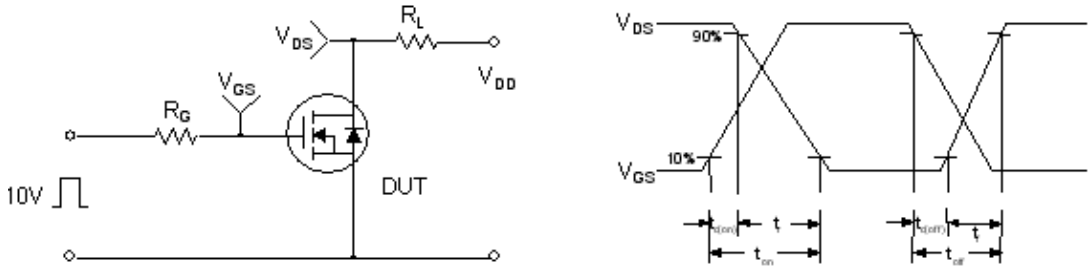


Figure 13. Resistive Switching Test Circuit & Waveforms

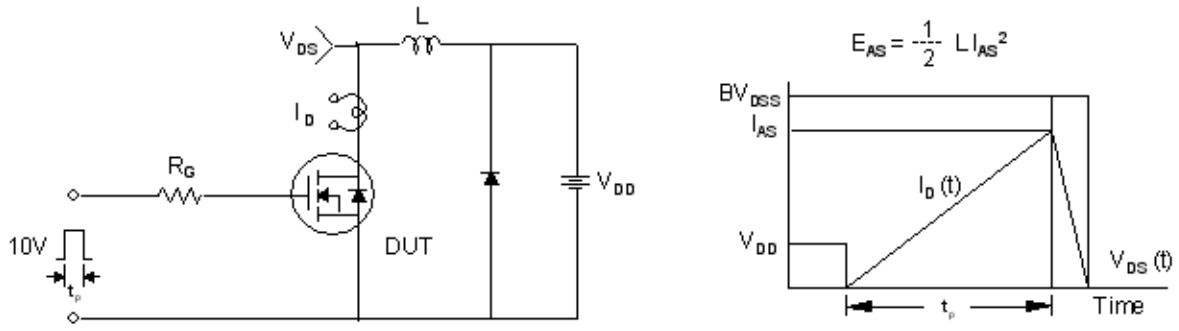


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

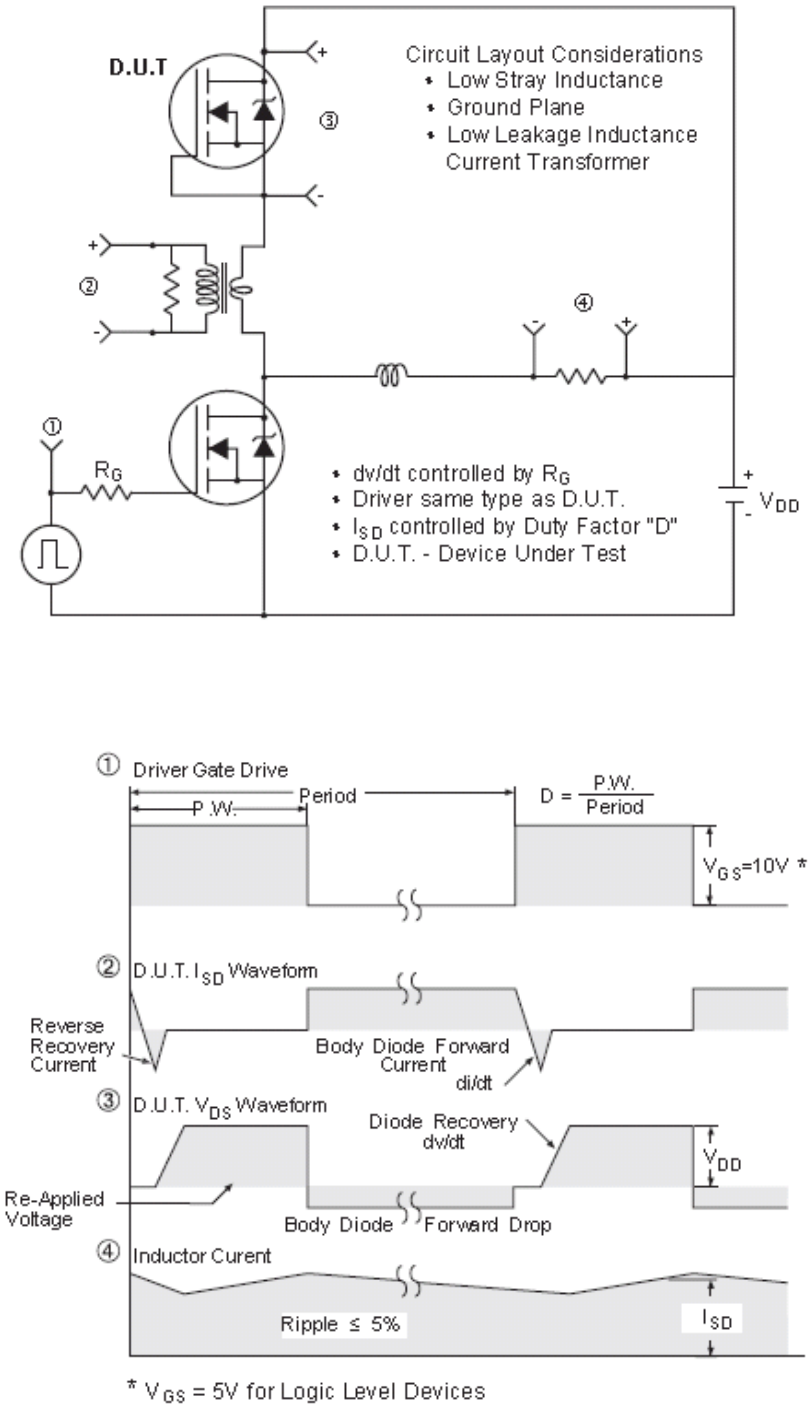


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms (For N-channel)